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Design of a Nanometric Reversible 4-Bit Binary Counter with Parallel Load

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Abstract: In recent years, reversible logic has considered as an efficient computing method having its applications in quantum computing, low power computing, nanotechnology and DNA computing. All of the Boolean functions can be implemented using reversible gates. In this paper, we propose a reversible 4-Bit binary counter with parallel load. It has minimum complexity and quantum cost considerably. The proposed circuit is the first attempt of designing a 4-Bit binary counter with parallel load. Counter is essentially a register that goes through a predetermined sequence of states. The reversible gates in the counter are connected in such a way as to produce the prescribed sequence of binary states. This counter receives a 4-Bit data from input and delivers data to D Flip Flop in next cycle. Loading data from input is determined with Load property. The important reversible gates used for our reversible logic synthesis are Feynman gate, Peres gate and Fredkin gate. The proposed circuit becomes a robust design by our optimal method and using these gates. The proposed circuit has minimum number of the garbage outputs and constant inputs in reversible circuit. The proposed circuit is the first attempt and efficient state for a nanometric reversible 4-Bit binary counter. More complex systems could be constructed using the proposed circuit.

Key words: Reversible Binary Counter, Parallel Load, Reversible Logic, Nanometric Scale, D Flip Flop, Quantum Computing, Nanotechnology.

INTRODUCTION

There are some of the goals in VLSI circuit design. One of these goals is reduction of power dissipation. In the early 1960s, R. Landaur presented that irreversible hardware computation is one of the reasons in energy dissipation ultimate to information loss (Landauer, 1961). There is zero internal power dissipation in the reversible logic circuits because information is not losed in its circuit. Bennett presented that reversible logic gates can avoid KTIn2 energy dissipation in a logic circuit (Bennett, 1973). In reversible logic gates or circuits, number of inputs is equal to number of outputs. Outputs can be determined from amount of inputs (Kerntopf, 2004; Perkowski, *et al,* 2001; Perkowski, 2001).

Reversible gates have applications in quantum computing, low power computing, low power CMOS design, optical computing, optimal information processing, nanotechnology and DNA computing.

Quantum computing theory is basis of quantum gates. Reversible state of Quantum mechanical system is foundation of reversible quantum circuits. The 1×1 and 2×2 quantum gates are introduced in some quantum techniques (Kaye, 2007). We use from 1×1 and 2×2 quantum gates to implement the bigger gates like 3×3 quantum gate. Number of the 1×1 and 2×2 gates is quantum cost (QC) of a reversible or quantum circuit. Number of gates (NOG), number of constant inputs (Gin), number of garbage outputs (Gout), number of transistors and quantum cost are major factors of complexity in reversible logic design (Maslov, 2003; Haghparast, 2008; Haghparast, 2007; Haghparast, 2008; Haghparast, 2008; Haghparast, 2009). The quantum cost is an important factor for evaluating a circuit design (Gupta, 2006; Mohammadi, 2009). One of the major problems of reversible gates is that Fan-out is not allowed (Perkowski, 2001; Vasudevan, 2004).

Traditional irreversible logic circuits were more simplex circuits than quantum or reversible logic circuits. Reversible logic has efficient characteristic that constructs the circuits as a optimal design. The Conventional circuits if different with synthesis of a reversible logic circuit. Some of the reversible logic circuits are synthesized and optimized by genetic algorithms (Lukac, 2003; Mohammadi, 2007; Mohammadi, 2008).

A reversible logic circuit should use the below features (Perkowski, 2001):

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- Minimum number of reversible gates.
- Minimum number of garbage outputs.
- Minimum constant inputs.
- Keep the length of cascading gates minimum.

Garbage output is some of the inputs that are not used for further computations (Thapliyal Himanshu, 2005). Constant input is some of the inputs that are added to an nxk function. It cause to make the circuits as reversible state (Saiful Islam, 2005). A circuit with flip-flops is considered a sequential circuit even in the absence of combinational logic. Circuits that include flip-flops are usually classified by the function of them.

Counter is essentially a register that goes through a predetermined sequence of states. The gates in the counter are connected in such a way as to produce the prescribed sequence of binary states. These gates construct a counter circuit.

A counter with parallel load can be used to create any desired count sequence. A 4-bit counter with parallel load can be used to generate a BCD count in two ways:
Using the load input: Overview of this design is shown in Fig. 1.
Using the clear input: Overview of this design is shown in Fig. 2.

2. Background:

Reversible Logic:

In this section, we describe the structure and functionality of reversible gates that are used in our design. Some of the reversible gates are described to compare with other studies. Finally, we will discuss about quantum gates.

There is a one-to-one correspondence between the inputs and the outputs. Thus an n-input n-output function F is reversible. In this logic, the input vector will be determined from the output vector. Some of the technologies such as CMOS, nanotechnology and optical circuits can implement primary reversible logic gates.

Reversible Logic Gates:

An nxn reversible gate can be shown as below form:

$I_v = (I_1, I_2, I_3, \ldots, I_n)$
$O_v = (O_1, O_2, O_3, \ldots, O_n)$

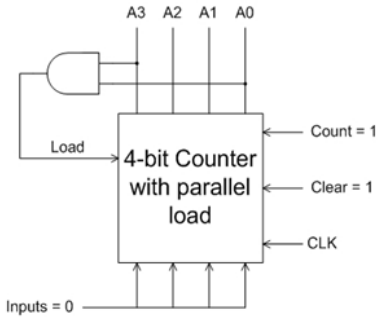

Fig. 1: 4-Bit Counter Using The Load Input.

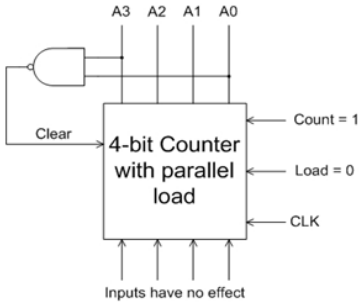

Fig. 2: 4-Bit Counter Using the Clear Input.

I_v and O_v are input and output vectors respectively. If there are n inputs in a circuit then exists 2^n reversible n n gates. A set of joined gates Construct the reversible circuit. These circuits have the parallel lines similar to the musical lines. In fact, the inputs or outputs of the circuit are formed of these lines. The gates are located on these parallel lines. Composition of the music pieces is a basis form that design and implement a reversible circuit. These gates have not same functional complexity and quantum cost. These efficient factors are variable and depend on the structures.

Several reversible logic gates have been proposed in the past years (Thapliyal Himanshu, 2005; Haghparast, 2008; Haghparast, 2007; Haghparast, 2008; Feynman, 1985; Fredkin, 1982; Peres, 1985; Khan, 2002; Azad Khan, 2002). Some of reversible gates are: Feynman gate, FG (Feynman, 1985), Toffoli gate, TG (Fredkin, 1982), Fredkin gate, FRG (Peres, 1985), Peres gate, PG (Khan, 2002), New gate, NG (Himanshu Thapliyal, 2006) and HNG gate, HNG (Haghparast, 2008). In this section, we review and describe these reversible logic gates. We will study the proposed circuit using them.

Feynman gate (FG): Feynman gate also known as controlled-not gate (1-CNOT). It is a 2×2 reversible gate that can be explained by the equations: P = A and Q = A⊕B, 'A' is a control bit and 'B' is the data bit. If control input bit is "1", the output bit (Q) is NOT of B; otherwise, it is B. If the B input be "0" then the output bits (P, Q) are equal to A. that is the Feynman gate can be used to copy a input bit. However, we can use the Feynman gate for copy a signal. In fact, it is a fan-out gate. Quantum cost of its circuit is 1. The Feynman gate can be presented as:

I_v = (A, B)
O_v = (P = A, Q = A⊕B)

I_v and O_v are input and output vectors respectively. The Feynman gate is shown in Fig. 3.

Toffoli gate (TG): Toffoli gate also known as controlled controlled-not gate (CCNOT). It is a 3×3 reversible gate that can be described by the equations: P = A, Q = B and R = AB⊕C. If the C input bit is "0", the R output bit is multiplier of the other input bits (A, B). this is a universal gate. The logical reversible circuits can be implemented by the Toffoli gate. The Toffoli gate can be described as:

I_v = (A, B, C)
O_v = (P = A, Q = B, R = AB⊕C)

I_v and O_v are input and output vectors respectively. The Toffoli gate is shown in Fig. 4.

Fredkin gate (FRG): Fredkin gate also known as controlled permutation gate. It is a 3×3 reversible gate that can be described by some of the equations.

It is a universal gate for circuit design and is directly onto quantum logic gates. Quantum cost of its circuit is 5. FRG can be implemented by other gates.

Fig. 3: Feynman gate.

Fig. 4: Toffoli gate.

Fig. 5: Fredkin gate.

The Fredkin gate can be described as:

I_v = (A, B, C)
O_v = (P = A, Q = A'B⊕AC, R = A'C⊕AB)

I_v and O_v are input and output vectors respectively. Conservator property is one of the Fredkin gate characteristic. Its input vector has the hamming weight that is equal to hamming weight of its output vector. The Fredkin gate is shown in Fig. 5.

Peres gate (PG): Peres gate also known as New Toffoli Gate (NTG). It is constructed of Toffoli Gate and Feynman Gate. The Peres gate is also a 3×3 reversible gate. It is equal to the produced evolution by a Toffoli gate followed by a Feynman gate. The Peres gate is also universal gate. It is more sophisticated than the Toffoli gate. Its quantum cost is 4 that is less than quantum cost of the Toffoli gate. This gate can be used in synthesis of all reversible circuits. The Peres gate can be described as:

I_v = (A, B, C)
O_v = (P = A, Q = A⊕B, R = AB⊕C)

I_v and O_v are input and output vectors orderly. The Peres gate is shown in Fig. 6.

New gate (NG): New gate is a 3×3 reversible gate. Quantum cost of its circuit is 7. The Peres gate can be represented as:

I_v = (A, B, C)
O_v = (P = A, Q = AB⊕C, R = A'C'⊕B')

Where I_v and O_v are input and output vectors. If C is "0" then it is used as a multiplier circuit. The New gate is shown in Fig. 7.

HNG gate: HNG gate is a 4×4 reversible gate. Quantum cost of the HNG gate is 6. The HNG gate can be explained as:

I_v = (A, B, C, D)
O_v = (P = A, Q = B, R = A⊕B⊕C, S = (A⊕B).C⊕AB⊕D)

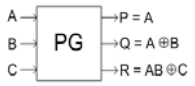

Fig. 6: Peres gate.

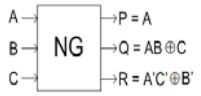

Fig. 7: New gate.

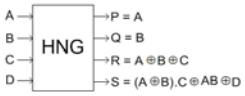

Fig. 8: HNG gate.

Where I_v and O_v are input and output vectors orderly. This is a universal gate. The HNG gate can be used as a reversible full adder. Quantum cost of the HNG gate is 6. Thus, the quantum cost of the HNG full adder has minimum cost for a full adder circuit. In the other word, Peres full adder consist of two Peres gates. We can use also these two full adder circuits that construct a multiplier design. The HNG gate is shown in Fig. 8.

D Flip Flop: The reversible D Flip Flop consist of one Fredkin gate plus one Feynman gate which is later used to design the complex sequential circuits. It is a reversible Master-Slave D Flip Flop (Lukac, 2003). The D Flip Flop gate is shown in Fig. 9.

The characteristic equation of the D Flip Flop used one Fredkin gate plus one Feynman gate. The Feynman gate is used to copy the output bit. It has highly optimized in the number of reversible gates, constant inputs and garbage outputs. CP refers to the clock pulse. It can be easily verified that the constructions meets the desired characteristics of the positive edge triggered D Flip Flop. The feedback connection from output to input is necessary because the D Flip Flop does not have a “No Change” condition. The construction of the D Flip Flop is shown in Fig. 10.

Quantum cost (QC) of the D Flip Flop circuit is as:

$QC_{(D\text{-}FF)} = QC_{(FRG)} + QC_{(FG)} = 5 + 1 = 6$

3. 4-Bit Binary Counter with Parallel Load:

A 4-Bit binary counter with parallel load can be used to create any desired count sequence. It can be used to generate a BCD count. The capabilities of its circuit are shown in Fig. 11.

The operations of a 4-Bit binary counter are summarized in Table 1. When both of L and C inputs are "0" then any changes do not happen in the circuit. Count up characteristic is the major operation in its circuit.

Fig. 9: D Flip Flop gate.

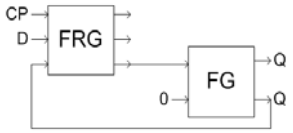

Fig. 10: Reversible Master-Slave D Flip Flop.

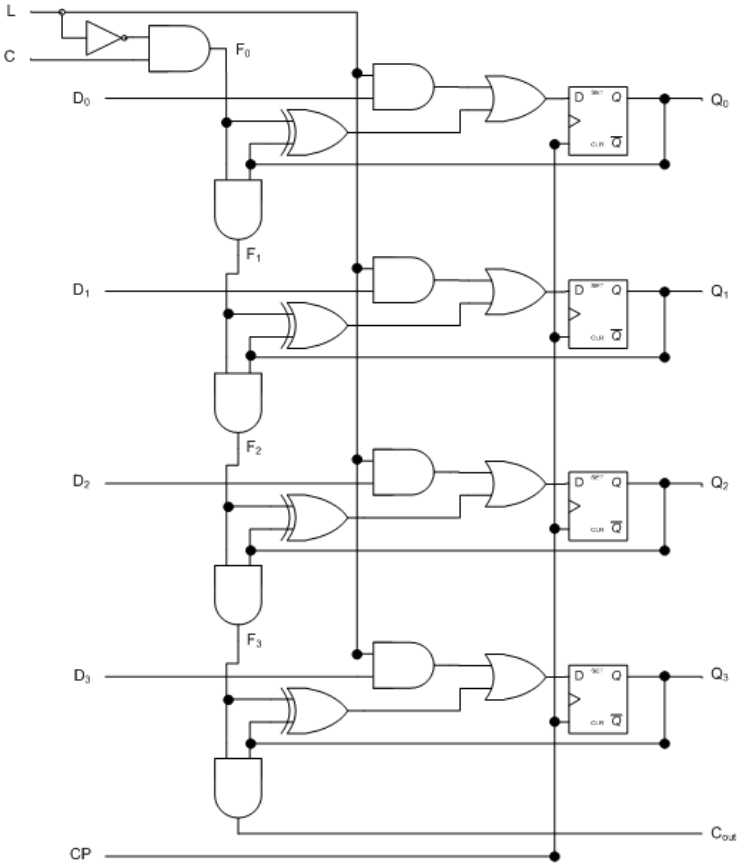

Fig. 11: 4-Bit Binary Counter with Parallel Load.

The counter starts with an all-zero output, and C input is always active. As long as the output of the AND gate is "0", each positive clock edge increments the counter by one. Equations and manipulations into forms containing XOR gates:

$F_0 = L'.C$
$Q_0 = (F_0 \oplus Q_0) + (L.D_0)$
$F_1 = F_0.Q_0$
$Q_1 = (F_1 \oplus Q_1) + (L.D_1)$
$F_2 = F_1.Q_1$

$Q_2 = (F_2 \oplus Q_2) + (L.D_2)$
$F_3 = F_2.Q_2$
$Q_3 = (F_3 \oplus_3) + (L.D_3)$
$C_{out} = F_3.Q_3$

4. Our Proposed Nanometric Reversible 4-Bit Binary Counter with Parallel Load:

The construction and operations of a 4-Bit binary counter with parallel load is shown in Fig. 12. The important reversible gates used for our reversible logic synthesis are Feynman gate, Peres gate and Fredkin gate.

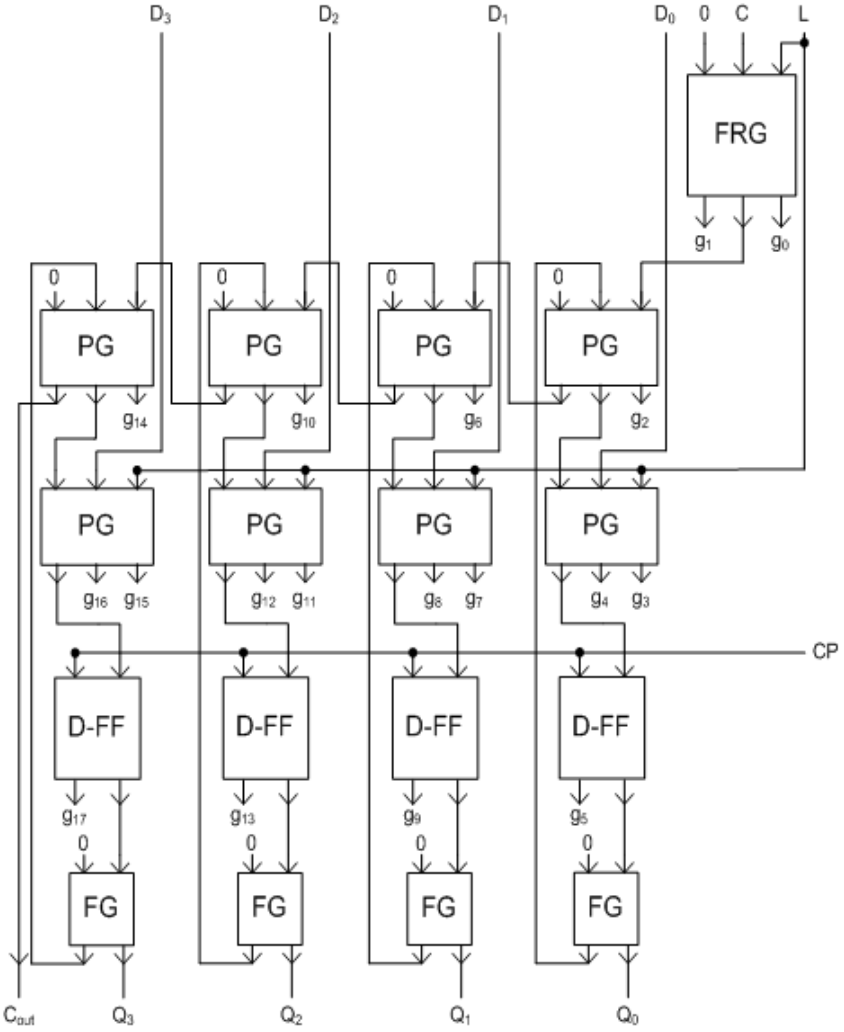

Fig. 12: A Reversible 4-Bit Binary Counter with Parallel Load.

This counter receives a 4-Bit data from input and delivers data to D Flip Flop in next cycle. Loading data from input is determined with L property. The proposed circuit is the first attempt of designing a 4-Bit binary counter with parallel load. It has minimum number of reversible gates, constant inputs and garbage outputs. Our proposed circuit has minimum value of the quantum cost.

The proposed reversible circuit has two sections. First, the computing operations are performed on inputs or feedback data. This section is constructed of the Peres gates and the Feynman gates. Second, D Flip Flop stores the entered data and then feedback them to the circuit inputs.

We have implemented the computing operations using Peres gate instead of the other gates because it cause to our proposed circuit be optimal. The Peres gate has some of the computation features with minimum quantum cost. We have performed XOR, AND, OR operations using Peres gates. in the second approach, we have used D Flip Flop to stores the entered or incremented data. In addition, it needs four Feynman gates to copy the outputs data and feedback them to the circuit inputs.

Table 1: Operations of 4-Bit Binary Counter with Parallel Load

CLK	L	C	Function
↑	0	0	No Change
↑	0	1	Count Next Binary State
↑	1	0	Load Inputs

5. Evaluation of the Proposed Reversible 4-Bit Binary Counter:

The proposed reversible circuit is the first attempt of design a 4-Bit binary counter with parallel load. Evaluation of the proposed circuit can be realized easily with the results in Table 2.

One of the major factors of a circuit is its hardware complexity. We can demonstrate that our reversible proposed circuit is the robust approach of a 4-Bit binary counter with parallel load. Let

α = A two input EX-OR gate calculation
β= A two input AND gate calculation
δ= A NOT gate calculation
T = Total logical calculation

Total logical calculation is the count of the XOR, AND, NOT logic in the output expressions. For example, Fredkin gate has two XORs, four ANDs and two NOTs in the output expressions.
Thus: $T_{(FRG)} = 2\alpha+ 4\beta+2\delta$.

Note, we are used the Feynman gate for making fan-out in the reversible circuit. We copy the outputs with Feynman gates when we need two equal output expressions. For example, Fredkin gate needs 1XOR + 2AND + 1NOT to produce (A'B$\oplus$AC). Then need 1XOR + 2AND + 1NOT to produce (A'C$\oplus$AB). Thus, total logic calculation of the Fredkin gate is: $T_{(FRG)} = (1\alpha+ 2\beta+1\delta) + (1\alpha+ 2\beta+1\delta) = 2\alpha+ 4\beta+2\delta$.

Table 2: Experimental results of our proposed reversible 4-bit binary counter with parallel load

No. of gates	No. of garbage output	Total quantum cost	No. of constant input	Total logic calculation
17	18	65	9	$26\alpha+ 12\beta+2\delta$

Total logical calculation of the proposed 4-Bit binary counter circuit is as:

$T_{(FRG)} = 2\alpha+ 4\beta+2\delta$
$T_{(PG)} = 16+ 8$

$T_{(FG)} = 8$
$T = 26\alpha+ 12\beta+2\delta$

The totalized T is a minimum calculation of the proposed circuit. Therefore, total logical calculation is proved it as a optimal state. On the other hand, our design has the best and efficient features with least complexity. It is the first attempt of design a reversible 4-Bit binary counter with parallel load.

One of the major factors in designing a reversible logic circuit is number of constant inputs. The constant input is added to an nxk function to make it as reversible gate. Our proposed reversible circuit requires 9 constant inputs. Thus, we can state that our design approach is a new reversible circuit and first attempt of existing design in term of number if constant inputs. Our proposed design becomes an optimal circuit because we use from minimum number of the reversible gates. Minimum number of reversible gate and optimal design of the circuit is some of the reasons for minimizing the constant inputs.

Some of the outputs in the reversible gates are not used that are named garbage output. They can used as a primary output or input to other gates. The least number of garbage outputs is one of the other main constraints in designing a reversible logic circuit. Our proposed reversible 4-Bit binary counter requires 18 garbage outputs. Thus, we can state that our design approach is the efficient design of the reversible circuit and the optimized existing design in term of number if garbage outputs.

The proposed reversible circuit requires 17 reversible logic gates. Number of them is the least number in design of the proposed circuit. Minimum number of the gates is one of the major factors in the reversible logic. It is a important item in a optimal circuit.

One of the major factors in designing a reversible logic circuit is total quantum cost. Quantum cost (QC) is a property for any reversible gate. Total quantum cost of a reversible circuit is totalized of the quantum costs of the applied reversible gates.
Total quantum cost of the proposed reversible circuit is as:

$QC_{(FRG)} = 1 * (5) = 5$
$QC_{(PG)} = 8 * (4) = 32$

$QC_{(D\text{-}FF)} = 4 * (6) = 24$
$QC_{(FG)} = 4 * (1) = 4$

Total quantum cost = $QC_{(FRG)} + QC_{(PG)} + QC_{(D\text{-}FF)} + QC_{(FG)} = 5 + 32 + 24 + 4 = 65$

From above discussion, we can summarize the mentioned reversible circuit is the first attempt and optimal state for a 4-Bit binary counter with parallel load.

6. Conclusion:

In this paper, we proposed a robust reversible circuit for a 4-Bit binary counter with parallel load. The proposed reversible circuit is the first attempt of designing the mentioned counter. It has minimum complexity and quantum cost considerably. Table 2 demonstrates that the proposed reversible circuit is a first attempt and efficient design in term of hardware complexity, constant inputs, garbage outputs and number of gates. However, restricts of the reversible circuits were avoided excellent. More complex systems could be also constructed using our proposed circuit.

Some of the techniques to reduce the constant inputs and garbage outputs might be possible. In addition, some other optimization techniques like genetic algorithm may be utilize to reduce the quantum cost of the circuit.

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